

Message Text

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ORIGIN EB-08

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C O N F I D E N T I A L STATE 065988

USOECN, EXCON

E.O. 11652: XGDS-1

TAGS: ESTC, COCOM, JA, PO

SUBJECT: JAPANESE PROCESS CONTROL SYSTEM TO POLAND--IL 2565

REF: COCOM DOC (77) 751

FOLLOWING IS TECHNICIAN'S EVALUATION SUBJECT CASE WHICH
CONTAINS SEVERAL QUESTIONS TO BE ANSWERED BY JAPANESE.
USDEL MAY NOTE THAT DUE TO CHANGE IN PERSONNEL HERE THIS
REPORT INADVERTANTLY OVERLOOKED. HOWEVER, WE WILL DO OUR
BEST EXPEDITE CASE WHEN ANSWERS RECEIVED.

1. PERFORMANCE CAPABILITY OF SYSTEM/PROCESSING DATA RATE

THE HIDIC 80 PROCESS CONTROL COMPUTER WAS DESIGNED BY THE
MANUFACTURER TO BE MODULARLY EXPANDABLE, SO AS TO PROVIDE
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A PERFORMANCE CAPABILITY WHICH RANGES FROM THAT OF A SINGLE
CPU SYSTEM TO A MAXIMUM OF A 16-CPU SYSTEM. THE HIDIC 80
BUS STRUCTURE (SPECIALLY) WAS DESIGNED TO SUPPORT A
MULTIPLE CPU ARCHITECTURE AND IS CHARACTERIZED BY MULTIPLE
CROSSBAR BUSES FOR COMMUNICATIONS WITH A COMMON MAIN
MEMORY, PERIPHERAL DEVICES, PROCESS CONTROL AND DIRECT
DIGITAL CONTROL EQUIPMENT. THE PARTICULAR HIDIC SYSTEM

PROPOSED FOR POLAND CONSISTS OF TWO CENTRAL PROCESSING UNITS COUPLED BY A HIGH SPEED COMMON MEMORY. THE ORGANIZATION OF THE DUAL CPU SYSTEM CLEARLY ALLOWS BOTH PROCESSING UNITS TO PERFORM SIMULTANEOUSLY WITH MINIMAL INTERFERENCE AND YIELDING A TOTAL PERFORMANCE CAPABILITY OF ABOUT 33.7 MB/S. THE DECISION TO LIMIT THE USE OF ONE PORTION OF SUCH A DUAL CPU CONFIGURATION TO STANDBY OPERATIONS FOR INCREASED RELIABILITY DOES NOT REDUCE THE PERFORMANCE CAPABILITY RATED IN TERMS OF IL 1565. THUS, U.S. TECHNICIANS BELIEVE THE PROPOSED SYSTEM SHOULD BE CONSIDERED ON THE BASIS OF THE ADDITIVE PERFORMANCE OF THE DUAL CPU, WHICH IN THIS CASE IS 33.7 MB/S.

2. IN VIEW OF THE MULTIPLE CPU CONFIGURATION, SIMULTANEOUS ACCESS TO BOTH FIXED HEAD DISC DRIVES IS POSSIBLE--WHICH RESULTS IN A TOTAL EFFECTIVE BIT TRANSFER RATE OF 4.36 MB/S. ALSO, ACCORDING TO THE APPLICABLE IL 1565, NOTE 7 DEFINITION OF TOTAL ACCESSES, ALL DIRECT ACCESS PERIPHERAL MEMORY DEVICES, WHETHER ACCESSABLE SEQUENTIALLY, CONCURRENTLY, OR SIMULTANEOUSLY ARE ADDITIVE IN SO FAR AS THE TOTAL NUMBER OF SYSTEMS ACCESSES ARE CONCERNED.

3. GRAPHIC CAPABILITY OF H-7845C AND H-7844C PROCESS CONTROL CRT DISPLAY DEVICES

ATTACHMENTS 2, 3 AND 4 PROVIDED IN REF (B) WERE NOT VERY CONFIDENTIAL

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HELPFUL IN DESCRIBING THE GRAPHIC CAPABILITY OF THESE DISPLAY DEVICES. IN THIS CONNECTION, U.S. TECHNICIANS WOULD LIKE TO HAVE ADDITIONAL DETAILS CONCERNING THE INCLUSION OF EITHER A POINT PLOTTING MECHANISM OR A VECTOR GENERATOR IN THE PROCESS CONTROL DISPLAY DEVICES. IF EITHER OF THESE LINE DRAWING FEATURES IS PROVIDED, ARE THEY HARDWARE, FIRMWARE OR SOFTWARE IMPLEMENTED?

ALSO, PLEASE CLARIFY WHETHER OR NOT THE PROPOSED REMOTE DISPLAY DEVICES INCLUDE INTERACTIVE KEYBOARDS OR OTHER INPUT MECHANISMS, OR, ARE THEY LIMITED TO PERFORMING MONITOR-ONLY OPERATIONS?

4. TOTAL EFFECTIVE BIT TRANSFER RATE OF REMOTE TERMINAL DEVICES

INDEPENDENT OF THE MODE OF TRANSMISSION, ANALOG OR DIGITAL IL 1565, NOTE 12(Q) DEFINES A REMOTE TERMINAL DEVICE AS EQUIPMENT CAPABLE OF RECEIVING SEQUENCES OF BINARY DIGITS OR ALPHANUMERIC CHARACTERS. AS EVIDENCED BY ATTACHMENTS 2, 3 AND 4 OF REF.(B), THE PROPOSED REMOTE DISPLAY DEVICES ARE CAPABLE OF ACCEPTING ALPHANUMERIC AND

DISPPPIGITAL DATA, AND THUS CONSTITUTE REMOTE TERMINAL
DEVICES IN ACCORDANCE WITH THE DEFINITION.

IN VIEW OF THE HIGH TOTAL EFFECTIVE BIT TRANSFER RATE OF
THESE REMOTE TERMINAL DEVICES, RELATIVE TO THE NOTE 12
LIMITS, REDUCTIONS SHOULD BE CONSIDERED. VANCE

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